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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,482	12/10/2003	Joon Hyeon Lee	123034-050047728	5381

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EXAMINER	
GURLEY, LYNNE ANN	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,482	LEE, JOON HYEON	
	Examiner	Art Unit	
	Lynne A. Gurley	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,7 and 9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7 and 9-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the amendment and remarks filed 10/13/05.

Currently, claims 1-4, 6-7 and 9-14 are pending.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The disclosure is objected to because of the following informalities: in the amendment filed 5/20/05, Applicant made changes to the specification to replace [0025] with [0025] and [0025] with [0026]. These changes are in error. It is suggested that Applicant meant to replace [0026] and [0027].

Appropriate correction is required.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claim 4 is objected to because of the following informalities: in line 2, "the" after "wherein" should be deleted. Appropriate correction is required.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-4, and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa (US 5,843,848, dated 12/1/98) in view of Brown et al. (US 6,541,320, dated 4/1/03) and further in view of Jang et al. (US 5,518,959, dated 5/21/96).

4. Yanagawa shows the method as claimed in figures 1-7 and corresponding text, as: a method of forming a metal line layer in a semiconductor device, comprising: depositing a diffusion barrier layer 3 (Ti/TiN), a metal layer (Al metal layer 4) and an anti reflection layer (TiON layer, column 12, lines 19-30; column 1, lines 14-27; column 3, lines 65-67; column 4, lines 1-17) on a semiconductor substrate 1; depositing and patterning a photosensitive material 5 (on the anti reflection layer); etching portions of the anti reflection layer and the metal layer using activated plasma and the photosensitive material as a mask (figure 7B), whereby portions of the sidewalls of the metal layer are over-etched by plasma ions (column 4, lines 18-31;

column 5, lines 4-9; column 7, lines 51-64); removing the photosensitive material; etching portions of the diffusion barrier layer. To dry-etch the antireflection layer, the metal layer and the diffusion barrier layer, Cl2/BCl3/N2 gas is discussed (column 8- column 12, line 48).

5. Yanagawa lacks anticipation only in not teaching that: 1) an insulating film is further is deposited on the anti reflection layer; 2) a side wall oxide film is formed on the over-etched side walls of the metal layer by reacting the metal layer with ozone; and the sidewall oxide film is Al2O3; 3) the antireflection layer is Ti/TiN; 4) portions of the diffusion barrier layer are etched using the insulating film as an etch mask; 5) the insulating film is a nitride film; and, 6) the insulating film is dry etched using activated plasma comprising a combination of CHF3/CF4/Ar or CxFx (where x, y are natural numbers)/O2/Ar gas.

6. Brown teaches an insulating hard mask used underneath and in combination with the resist and the anti reflection layer to pattern the metal layer. The mask may be a nitride (column 4, lines 35-57).

Jang teaches the formation of oxide sidewall spacers on a similar stack of metal layers, TiN/Al/TiN layers, for the purpose of improving the dielectric coverage of the metal stack in an interconnect.

It would have been obvious to one of ordinary skill in the art to have used an insulating film formed on the anti reflection layer and under the photosensitive material as a hard mask; and to have had the insulating layer be a nitride film, and to have etched portions of the diffusion barrier layer using the insulating film as an etch mask in the method of Yanagawa, with the motivation given in Brown that an insulating layer used as a hard mask layer, which may be a nitride, is conventional when used in conjunction with an antireflection layer. It increases the

accuracy of the etching step. Additonally, Ti/TiN is a conventional alternative to TiON as an antireflection layer (See Narita et al. US 6,383,942, col. 5, lines 39-41 for support).

It would have been obvious to one of ordinary skill in the art to have formed a side wall oxide film on the over-etched side walls of the metal layer by reacting the metal layer with ozone; and to have had the sidewall oxide film be Al2O3, in the method of Yanagawa, with the motivation that Jang teaches that for using the Al stack for conventional interconnection purposes, the ozone spacers promote improved step coverage of subsequently formed dielectric layers. When the Al is exposed to the ozone, Al2O3 is formed.

It would have been obvious to one of ordinary skill in the art to have had the insulating film be dry etched using activated plasma comprising a combination of CHF3/CF4/Ar or CxFx (where x, y are natural numbers)/O2/Ar gas, in the method of Yanagawa, with the motivation that these are well known metal etchants which would work alternatively, in combination, to etch the claimed metal stack.

7. Claims 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagawa (US 5,843,848, dated 12/1/98) in view of Jang et al. (US 5,518,959, dated 5/21/96).

8. Yanagawa shows the method as claimed in figures 1-7 and corresponding text, as: a method of forming a metal line layer in a semiconductor device, comprising: depositing a first and second (layer 3 Ti/TiN), and third (Al metal layer 4) conductive layer on a semiconductor substrate 1; depositing an insulating film (TiON/photoresist layer 5) on the third conductive layer (column 12, lines 19-30; column 1, lines 14-27. column 3, lines 65-67. column 4, lines 1-17; dry-etching portions of the insulating film, the third and the second conductive layers using activated

plasma, whereby portions of the sidewalls of the second conductive layer are over-etched by plasma ions (column 4, lines 18-31; column 5, lines 4-9; column 7, lines 51-64); etching portions of the first conductive layer using the insulating film as an etch mask. To dry-etch the antireflection layer, the metal layer and the diffusion barrier layer, Cl2/BCl3/N2 gas is discussed (column 8- column 12, line 48).

9. Yanagawa lacks anticipation only in not teaching that: 1) a side wall oxide film is formed on the sidewalls of the over-etched second conductive layer by reacting the second conductive layer with ozone; and the sidewall oxide film is Al2O3; 2) the third conductive layer is Ti/TiN; and, 3) the insulating film is dry etched using activated plasma comprising a combination of CHF3/CF4/Ar or CxFx (where x, y are natural numbers)/O2/Ar gas.

Jang teaches the formation of oxide sidewall spacers on a similar stack of metal layers, TiN/Al/TiN layers, for the purpose of improving the dielectric coverage of the metal stack in an interconnect.

It would have been obvious to one of ordinary skill in the art to have had the third conductive layer be Ti/TiN and to have used the photoresist by itself as the insulating layer, in the method of Yanagawa, with the motivation that the Ti/TiN is a conventional alternative to TiON as an antireflection layer (See Narita et al. US 6,383,942, col. 5, lines 39-41 for support).

It would have been obvious to one of ordinary skill in the art to have formed a side wall oxide film on the over-etched side walls of the metal layer by reacting the metal layer with ozone; and to have had the sidewall oxide film be Al2O3, in the method of Yanagawa, with the motivation that Jang teaches that for using the Al stack for conventional interconnection

purposes, the ozone spacers promote improved step coverage of subsequently formed dielectric layers. When the Al is exposed to the ozone, Al2O3 is formed.

It would have been obvious to one of ordinary skill in the art to have had the insulating film be dry etched using activated plasma comprising a combination of CHF3/CF4/Ar or CxFx (where x, y are natural numbers)/O2/Ar gas, in the method of Yanagawa, with the motivation that these are well known metal etchants which would work alternatively, in combination, to etch the claimed metal stack.

10. Claims 1-4, 6-7 and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narita et al. (US 6,383,942, dated 5/7/02) in view of Jang et al. (US 5,518,959, dated 5/21/96).

11. Narita shows the method as claimed in figures 1-23 and corresponding text, as: a method of forming a metal line layer in a semiconductor device, comprising: depositing a first, second and third (103a/b) conductive layer on a semiconductor substrate 101; depositing an insulating film (103c/104) on the third conductive layer; dry-etching portions of the insulating film, the third and the second conductive layers using activated plasma, whereby portions of the sidewalls of the second conductive layer are over-etched by plasma ions (figs. 3-4 and fig. 7 where there is a two step etch to decrease the undercut of the Al layer; col. 2-3); etching portions of the first conductive layer using the insulating film as an etch mask. To dry-etch the antireflection layer, the metal layer and the diffusion barrier layer, Cl2/BCl3/N2 gas is discussed. An insulation film is deposited after the etching steps (105/18).

12. Narita lacks anticipation only in not teaching that: 1) a side wall oxide film is formed on the sidewalls of the over-etched second conductive layer by reacting the second conductive layer

with ozone; and the sidewall oxide film is Al2O3; 2) the third conductive layer is Ti/TiN; and, 3) the insulating film is dry etched using activated plasma comprising a combination of CHF3/CF4/Ar or CxFx (where x, y are natural numbers)/O2/Ar gas.

Jang teaches the formation of oxide sidewall spacers on a similar stack of metal layers, TiN/Al/TiN layers, for the purpose of improving the dielectric coverage of the metal stack in an interconnect.

It would have been obvious to one of ordinary skill in the art to have had the third conductive layer be Ti/TiN and to have used the photoresist by itself as the insulating layer, in the method of Narita, with the motivation that the Ti/TiN is a conventional alternative to TiON as an antireflection layer (See Narita et al. US 6,383,942, col. 5, lines 39-41 for support).

It would have been obvious to one of ordinary skill in the art to have formed a side wall oxide film on the over-etched side walls of the metal layer by reacting the metal layer with ozone; and to have had the sidewall oxide film be Al2O3, in the method of Narita, with the motivation that Jang teaches that for using the Al stack for conventional interconnection purposes, the ozone spacers promote improved step coverage of subsequently formed dielectric layers. When the Al is exposed to the ozone, Al2O3 is formed.

It would have been obvious to one of ordinary skill in the art to have had the insulating film be dry etched using activated plasma comprising a combination of CHF3/CF4/Ar or CxFx (where x, y are natural numbers)/O2/Ar gas, in the method of Narita, with the motivation that these are well known metal etchants which would work alternatively, in combination, to etch the claimed metal stack.

Response to Arguments

13. Applicant's arguments with respect to claims 1-4, 6-7 and 9-14 have been considered but are moot in view of the new ground(s) of rejection.

Prior Art Of Record

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Also, see Lo (US 5,726,102, previously cited) for same etchants, metal stack and overetch step. See **Gabriel** (US 5,462,892) for W/Ti/AL/W/Ti structure with oxidized Al (from any conventional oxygen source to produce Al2O3) to protect the wafer surface from acidic corrosion upon subsequent exposure to the atmosphere. See Jang et al. (US 5,599,740) and Nakamura et al. (US 4,798,650) for similar processes and undercuts of Al. Also, see the other art listed as being pertinent on the PTO Form 892.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

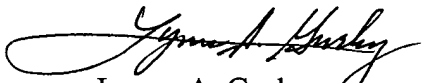
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lynne A. Gurley whose telephone number is 571-272-1670. The examiner can normally be reached on M-F 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Lynne A. Gurley
Primary Patent Examiner
TC 2800, Art Unit 2812

LAG
January 19, 2006